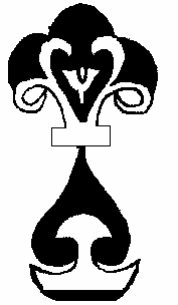
UNIVERSITÉ PARIS 12 VAL de MARNE

FACULTÉ DES SCIENCES ET TECHNOLOGIE

Bus I2C



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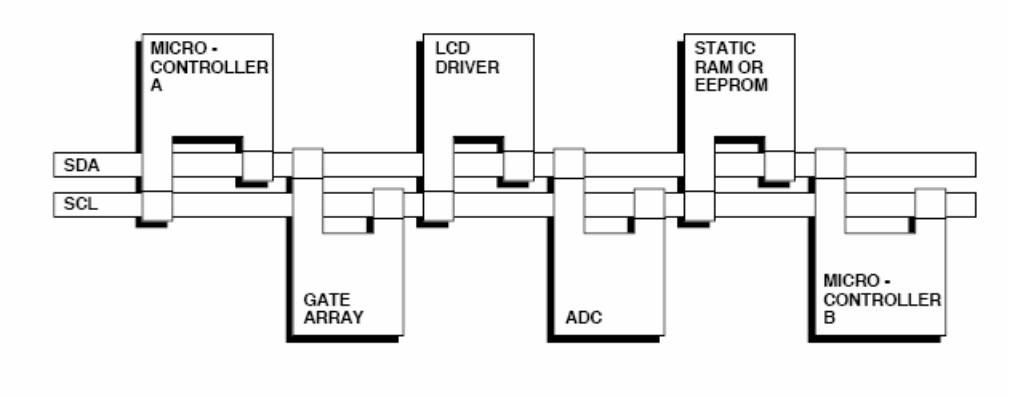
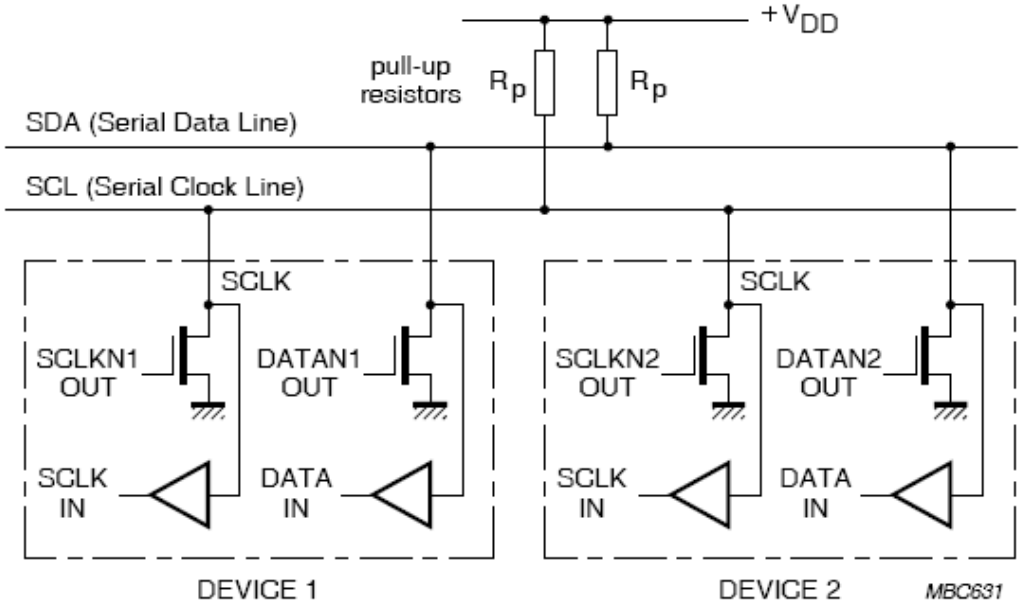
Structure du bus





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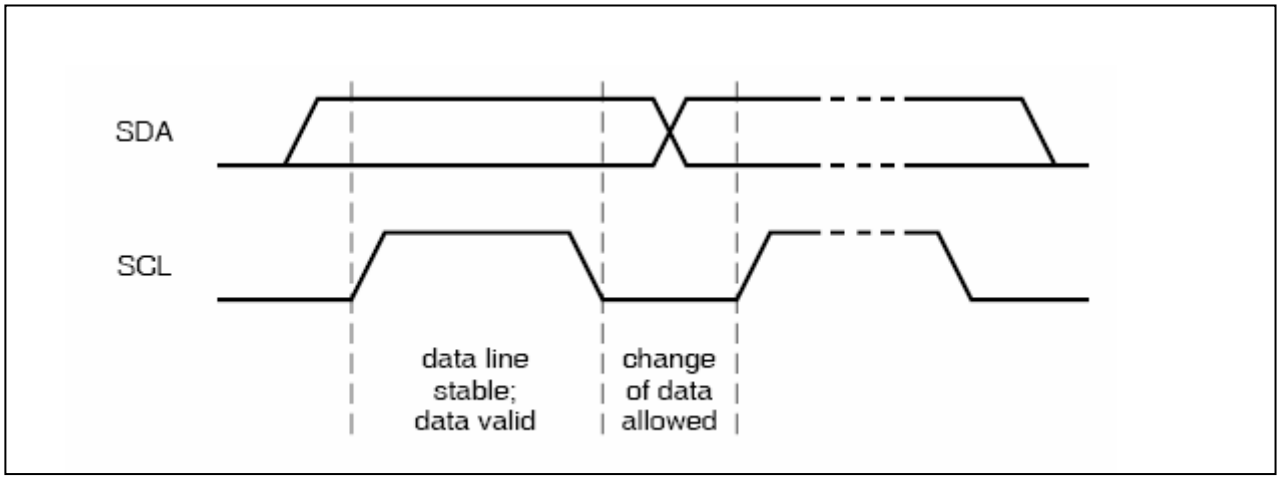
Définition des niveaux



PARAMETER	SYMBOL	STANDARD-MODE	
		MIN.	MAX.
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 –0.5 –0.5	 1.5 $0.3V_{DD}$
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 (2) (2)

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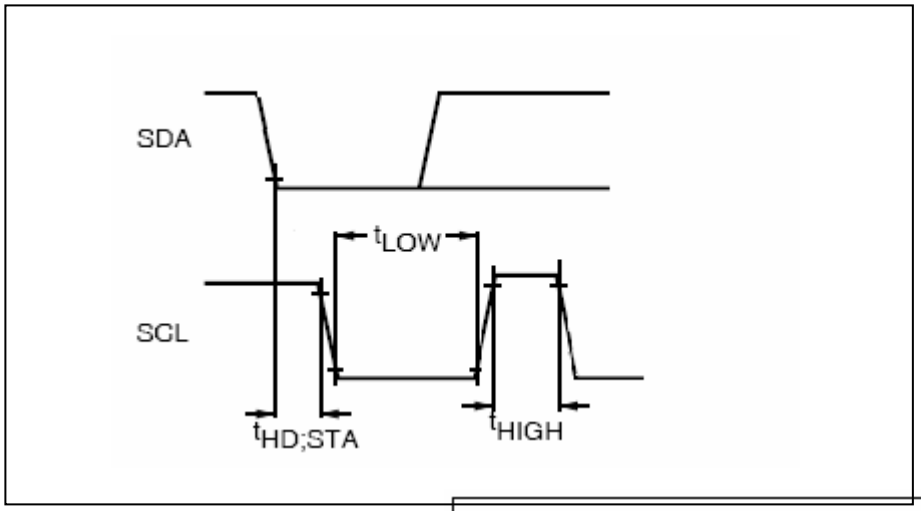
Définition des signaux d'horloge



PARAMETER	SYMBOL	STANDARD-MODE	
		MIN.	MAX.
SCL clock frequency	f_{SCL}	0	100
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–
LOW period of the SCL clock	t_{LOW}	4.7	–
HIGH period of the SCL clock	t_{HIGH}	4.0	–

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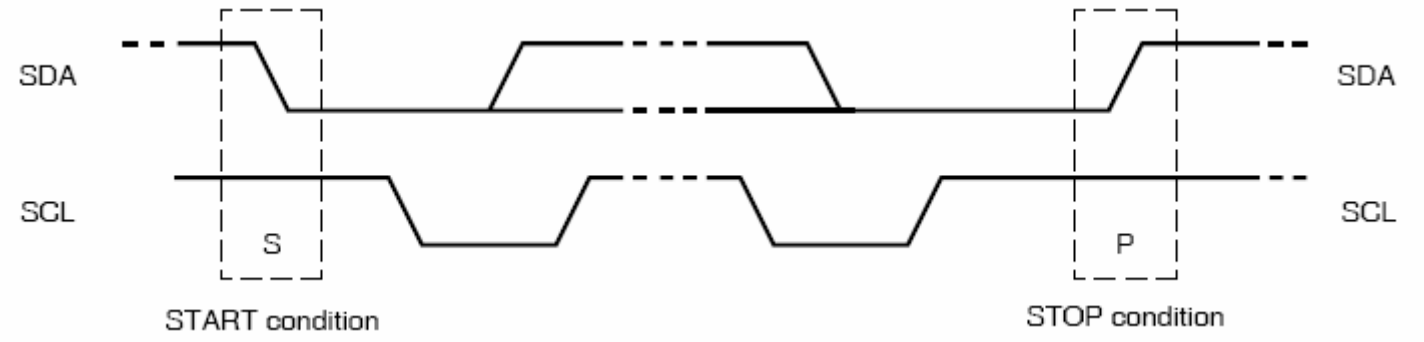
Protocole – Accès au bus



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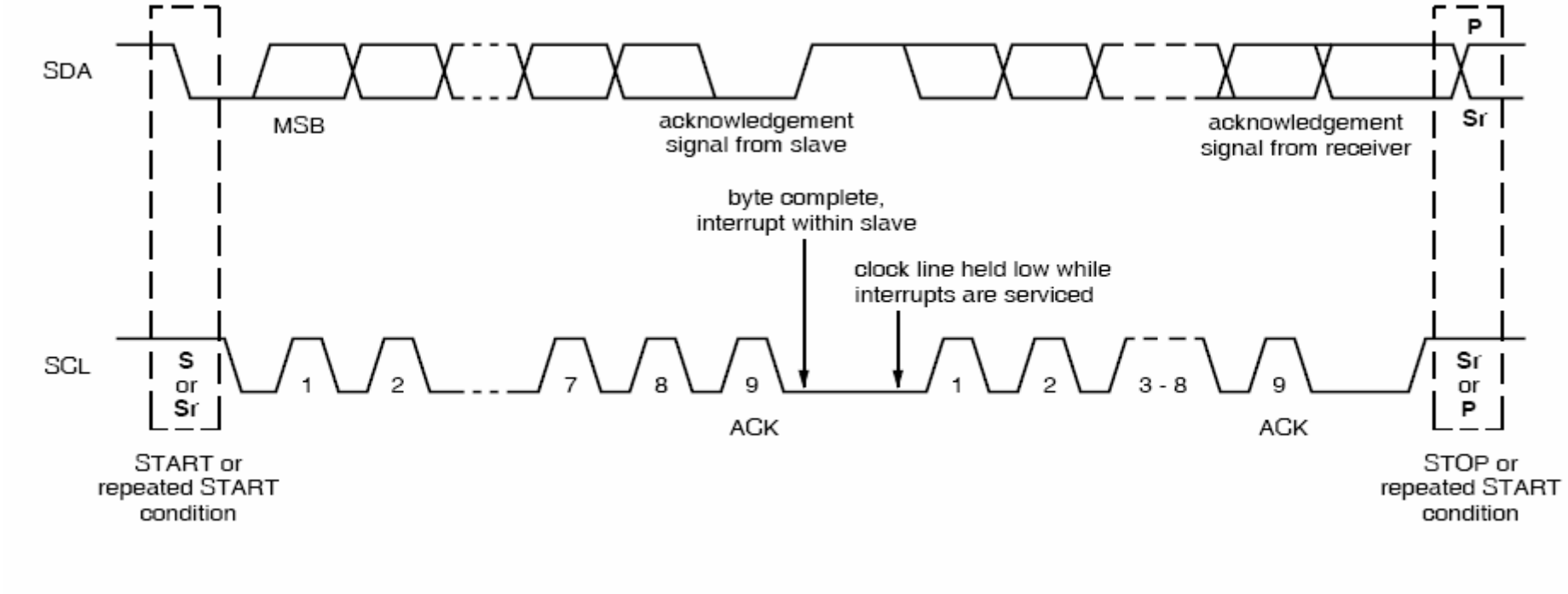
Protocole – Transmission d'une donnée



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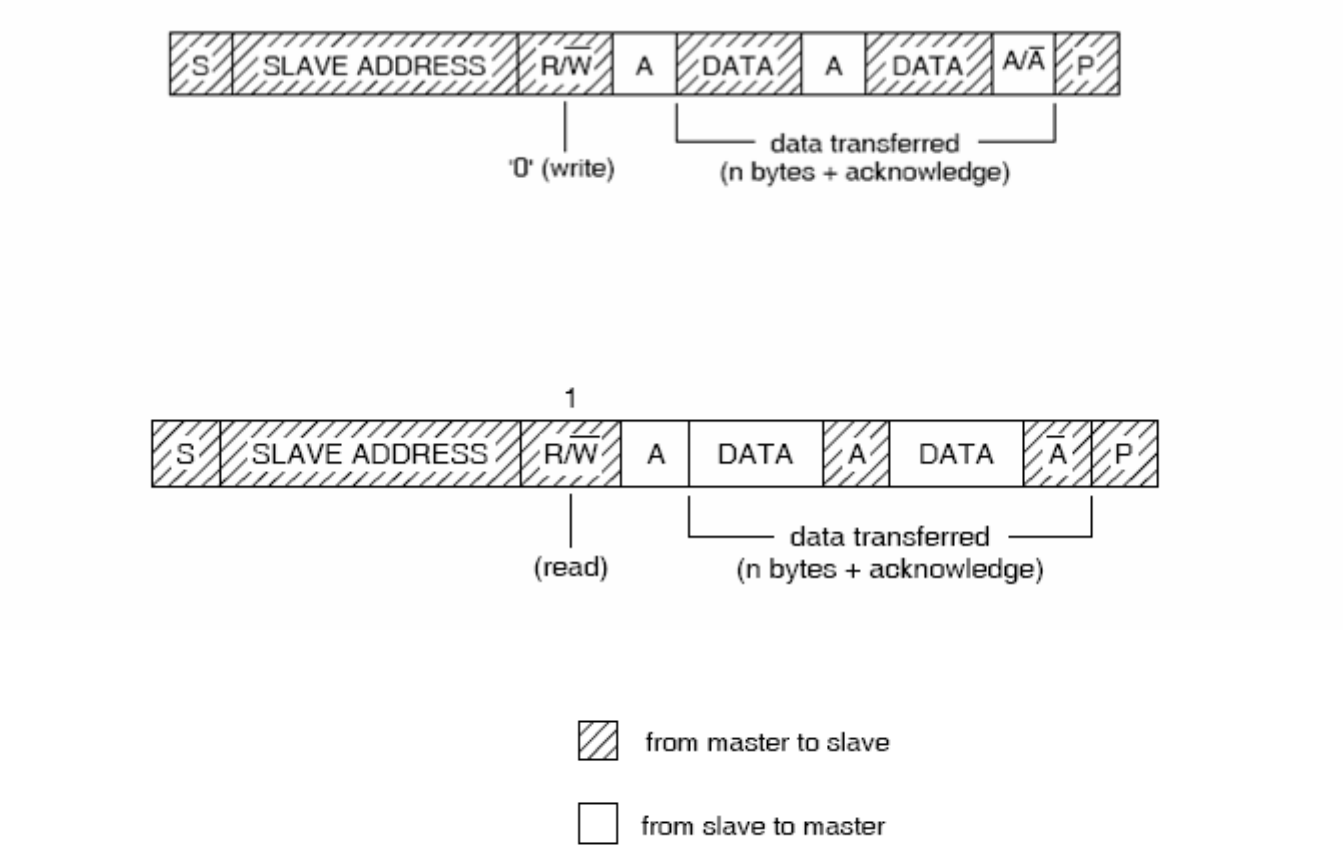
Protocole – Adressage 7 bits



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Protocole – Adressage 7 bits
Format de l'adresse

SLAVE ADDRESS	R/$\overline{W}$ BIT	DESCRIPTION
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

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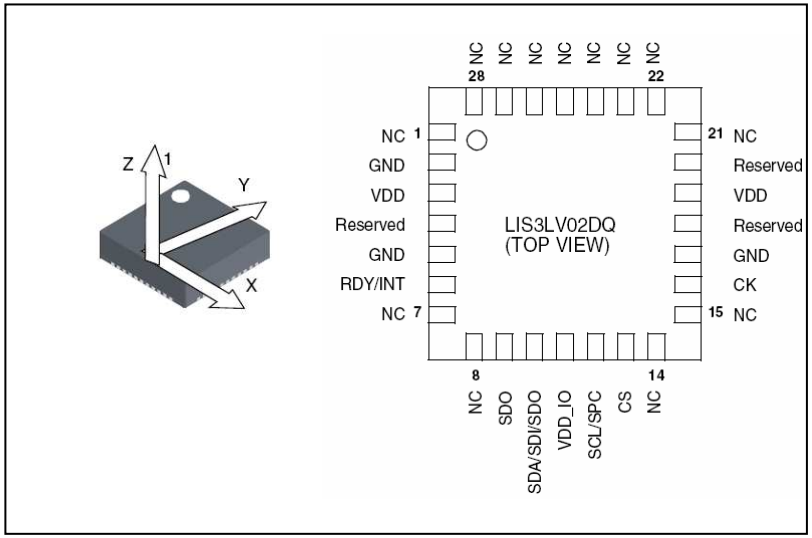
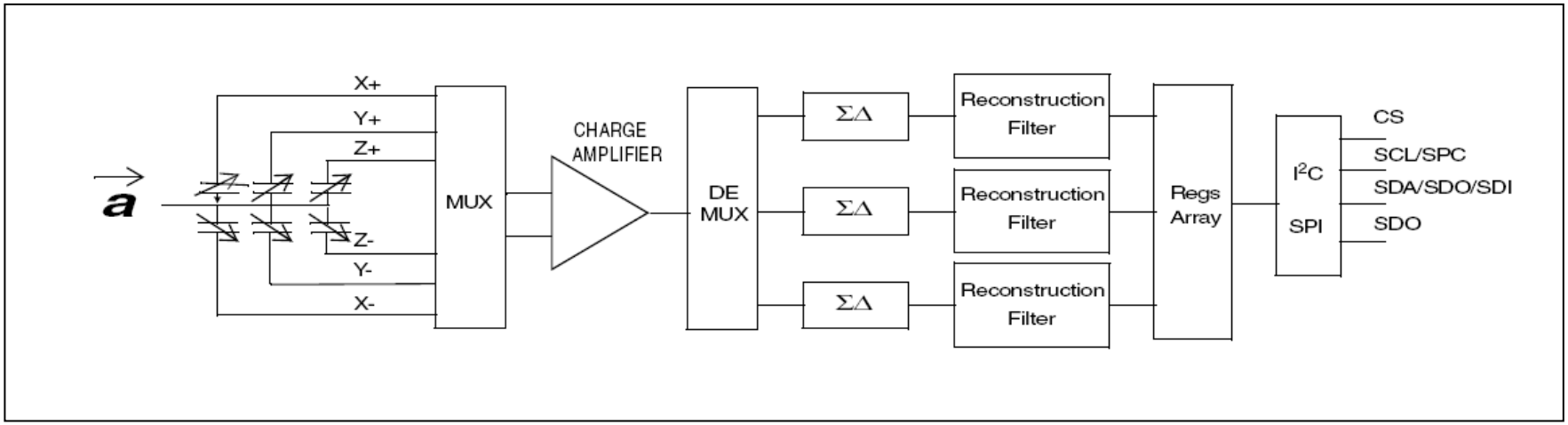
Mise en œuvre d'une centrale inertielle sur I2C
Etude du capteur LIS3LV02DQ





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Mise en œuvre d'une centrale inertielle sur I2C
Transfert I2C du capteur LIS3LV02DQ (suite)

Maître	ST	SAD + W		SUB		DATA		SP
Esclave			AK		AK		AK	

Maître	ST	SAD + W		SUB		SR	SAD + R			AK
Esclave			AK		AK			AK	DATA	

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Mise en œuvre d'une centrale inertielle sur I2C
Registre du capteur LIS3LV02DQ

Reg. Name	Type	Register Address	
		Binary	Hex
	rw	0000000 - 0001110	00 - 0E
WHO_AM_I	r	0001111	0F
	rw	0010000 - 0010101	10 - 15
OFFSET_X	rw	0010110	16
OFFSET_Y	rw	0010111	17
OFFSET_Z	rw	0011000	18
GAIN_X	rw	0011001	19
GAIN_Y	rw	0011010	1A
GAIN_Z	rw	0011011	1B
		0011100 -0011111	1C-1F
CTRL_REG1	rw	0100000	20
CTRL_REG2	rw	0100001	21
CTRL_REG3	rw	0100010	22
HP_FILTER RESET	r	0100011	23
		0100100-0100110	24-26
STATUS_REG	rw	0100111	27
OUTX_L	r	0101000	28
OUTX_H	r	0101001	29
OUTY_L	r	0101010	2A

Reg. Name	Type	Register Address		Default
		Binary	Hex	
OUTY_H	r	0101011	2B	output
OUTZ_L	r	0101100	2C	output
OUTZ_H	r	0101101	2D	output
	r	0101110	2E	
		0101111	2F	
FF_WU_CFG	rw	0110000	30	00000000
FF_WU_SRC	rw	0110001	31	00000000
FF_WU_ACK	r	0110010	32	dummy
		0110011	33	
FF_WU_THS_L	rw	0110100	34	00000000
FF_WU_THS_H	rw	0110101	35	00000000
FF_WU_DURATION	rw	0110110	36	00000000
		0110111	37	
DD_CFG	rw	0111000	38	00000000
DD_SRC	rw	0111001	39	00000000
DD_ACK	r	0111010	3A	dummy
		0111011	3B	
DD_THSI_L	rw	0111100	3C	00000000
DD_THSI_H	rw	0111101	3D	00000000
DD_THSE_L	rw	0111110	3E	00000000
DD_THSE_H	rw	0111111	3F	00000000
		1000000-1111111	40-7F	

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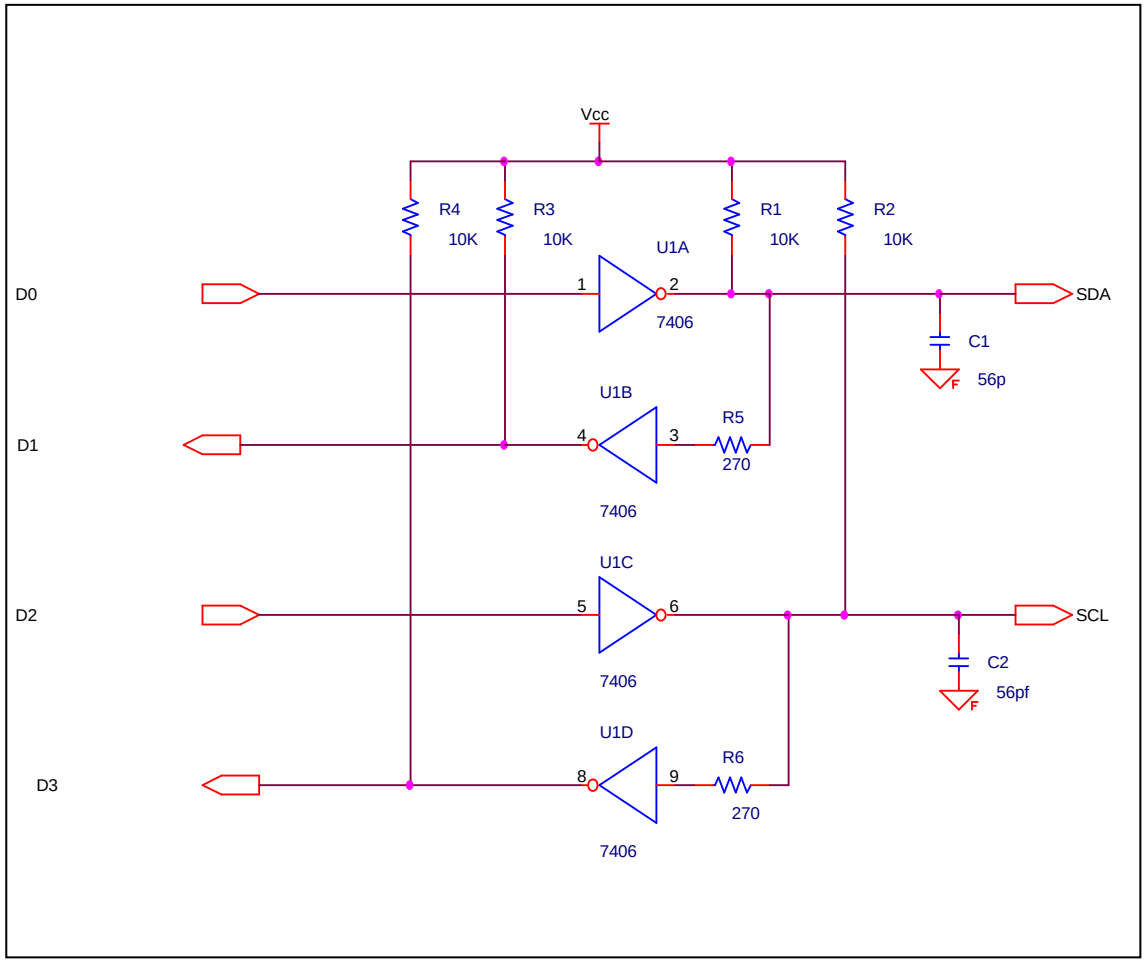
Mise en œuvre d'une centrale inertielle sur I2C
Interface PC I2C – 1ere méthode

connecteur SUB-D 25	Fonction	Direction	Registre
1	Strobe	S	contrôle
2	donnée D0	E/S	donnée
3	donnée D1	E/S	donnée
4	donnée D2	E/S	donnée
5	donnée D3	E/S	donnée
6	donnée D4	E/S	donnée
7	donnée D5	E/S	donnée
8	donnée D6	E/S	donnée
9	donnée D7	E/S	donnée
10	Acknowledge	E	état
11	Busy	E	état
12	Paper end	E	état
13	Select	E	état
14	Autofeed	S	contrôle
15	Error	E	état
16	Initialize	S	contrôle
17	Select input	S	contrôle
18-25	Ground		



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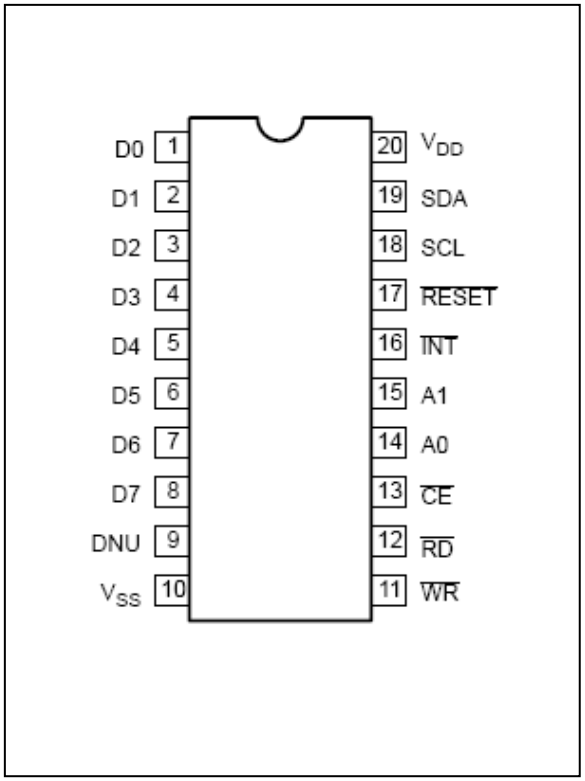
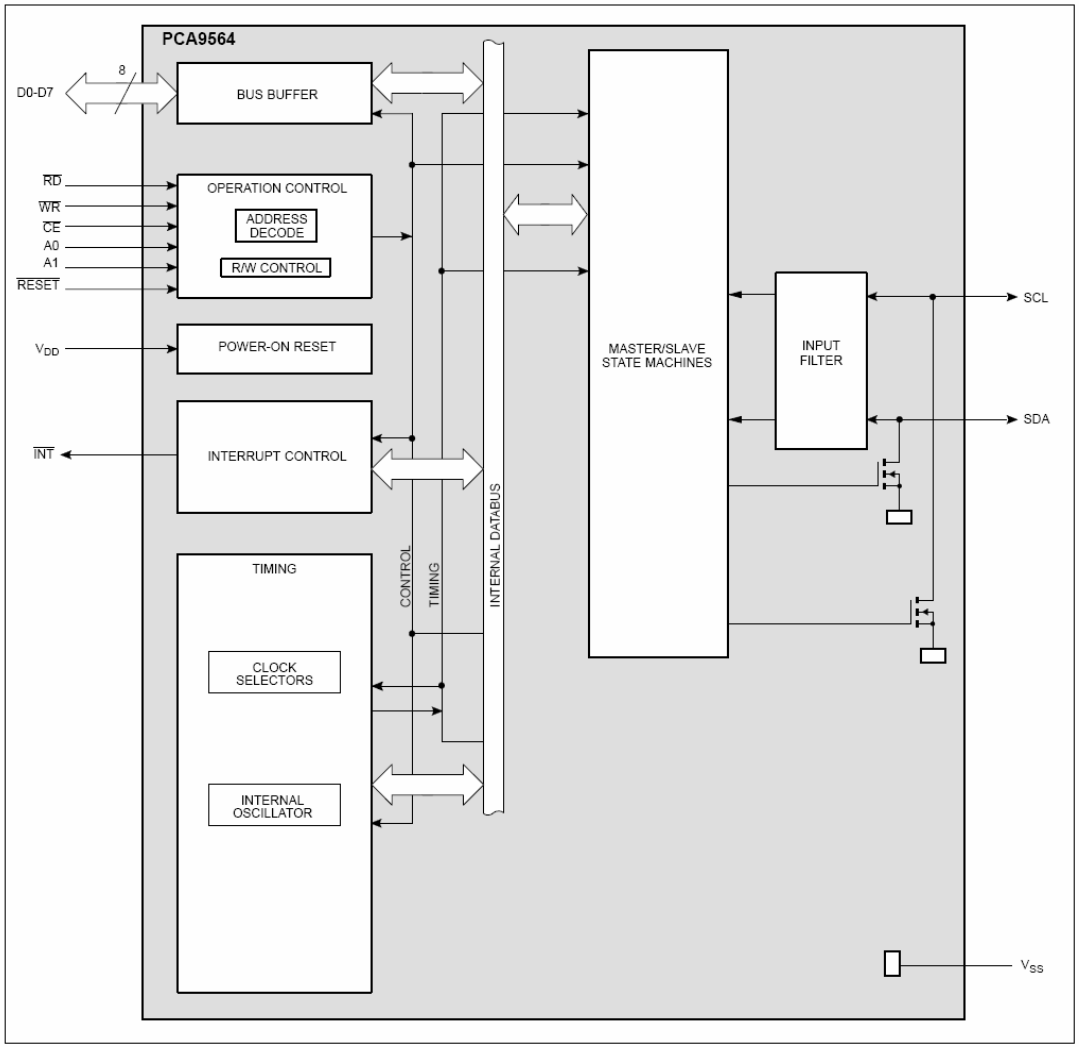
Mise en œuvre d'une centrale inertielle sur I2C
Interface PC I2C – 2ieme méthode
Circuit PCA 9564





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Mise en œuvre d'une centrale inertielle sur I2C
Interface PC I2C – 2ieme méthode
Circuit PCA 9564 – Registre interne

Nom	R/W	A1	A0	Registres							
				7	6	5	4	3	2	1	0
I2CSTA	R	0	0	BIT7	BIT6	BIT5	BIT4	BIT3	0	0	0
				7	6	5	4	3	2	1	0
I2CCTO	W	0	0	TE	TO6	TO5	TO4	TO3	TO2	TO1	TO0
				7	6	5	4	3	2	1	0
I2CDAT	R/W	0	1	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
				7	6	5	4	3	2	1	0
I2CADR	R/W	1	0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	0
				7	6	5	4	3	2	1	0
I2CCON	R/W	1	1	AA	ENSIO	STA	STO	SI	CR2	CR1	CR0

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Mise en œuvre d'une centrale inertielle sur I2C
Interface PC I2C – 2ieme méthode
Circuit PCF 9564 – Etat du composant

STATUS CODE (I2CSTA)	STATUS OF THE I^2C BUS AND SIO HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO HARDWARE
		TO/FROM I2CDAT	TO I2CCON				
			STA	STO	SI	AA	
08H	A START condition has been transmitted	Load SLA+W	X	X	0	X	SLA+W will be transmitted; ACK bit will be received
C0H	Data byte in I2CDAT has been transmitted; NOT ACK has been received	No I2CDAT action or	0	X	0	0	Switched to not addressed SLV mode; no recognition of own SLA
		no I2CDAT action or	0	X	0	1	Switched to not addressed SLV mode; Own SLA will be recognized
		no I2CDAT action or	1	X	0	0	Switched to not addressed SLV mode; no recognition of own SLA. A START condition will be transmitted when the bus becomes free
		no I2CDAT action	1	X	0	1	Switched to not addressed SLV mode; Own SLA will be recognized. A START condition will be transmitted when the bus becomes free.
C8H	Last data byte in I2CDAT has been transmitted (AA = 0); ACK has been received	No I2CDAT action or	0	X	0	0	Switched to not addressed SLV mode; no recognition of own SLA
		no I2CDAT action or	0	X	0	1	Switched to not addressed SLV mode; Own SLA will be recognized
		no I2CDAT action or	1	X	0	0	Switched to not addressed SLV mode; no recognition of own SLA. A START condition will be transmitted when the bus becomes free
		no I2CDAT action	1	X	0	1	Switched to not addressed SLV mode; Own SLA will be recognized. A START condition will be transmitted when the bus becomes free

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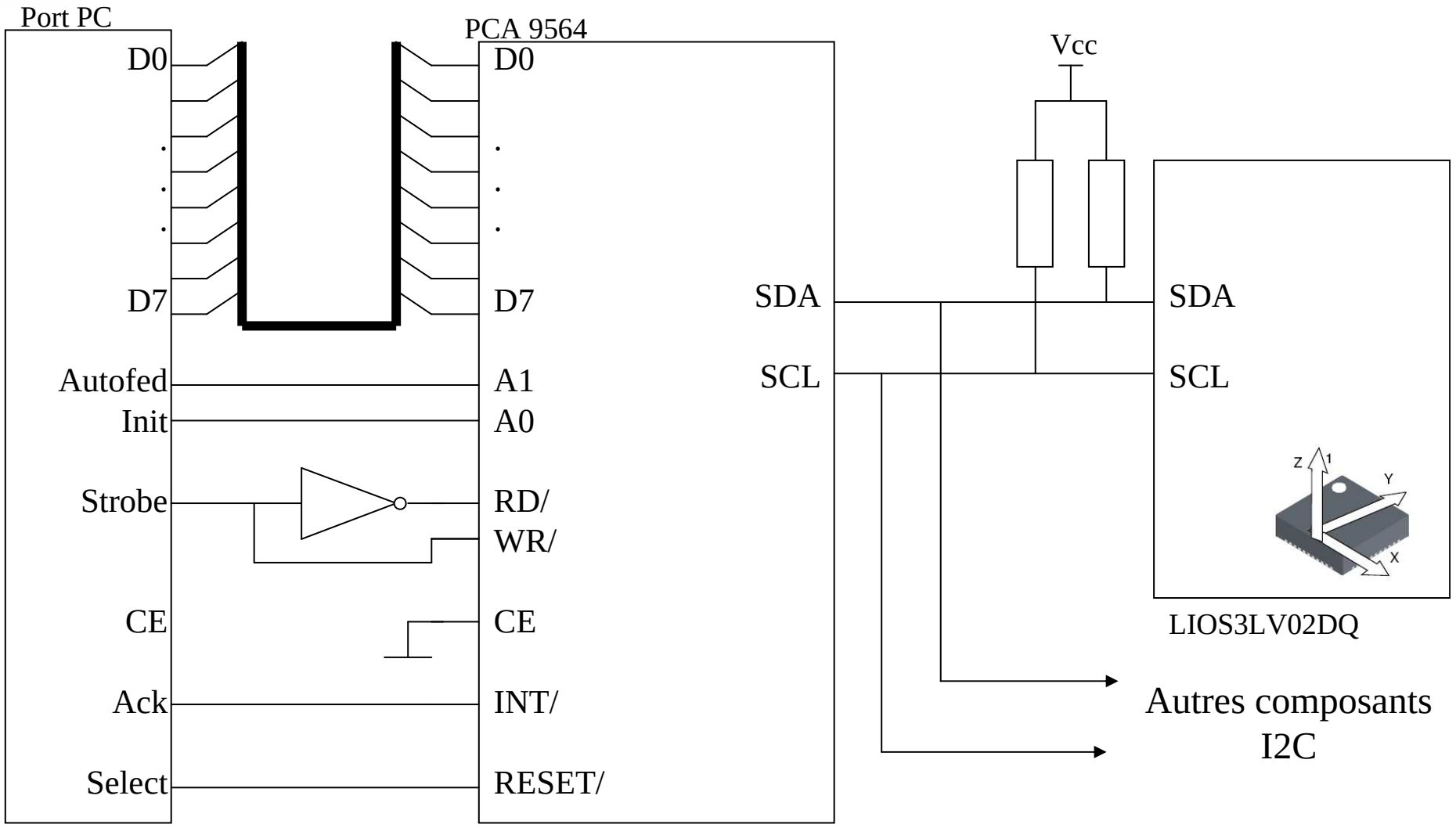
Mise en œuvre d'une centrale inertielle sur I2C
Schéma de principe



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Conclusion

- Simple à mettre en œuvre
- Destiné à des applications « petite distance »
- Composant dédiés
- Application contrôle commande

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