UNIVERSITÉ PARIS 12 VAL de MARNE

FACULTÉ DES SCIENCES ET TECHNOLOGIE

La liaison série EIA 232

Ph. Meyne

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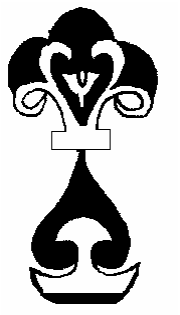
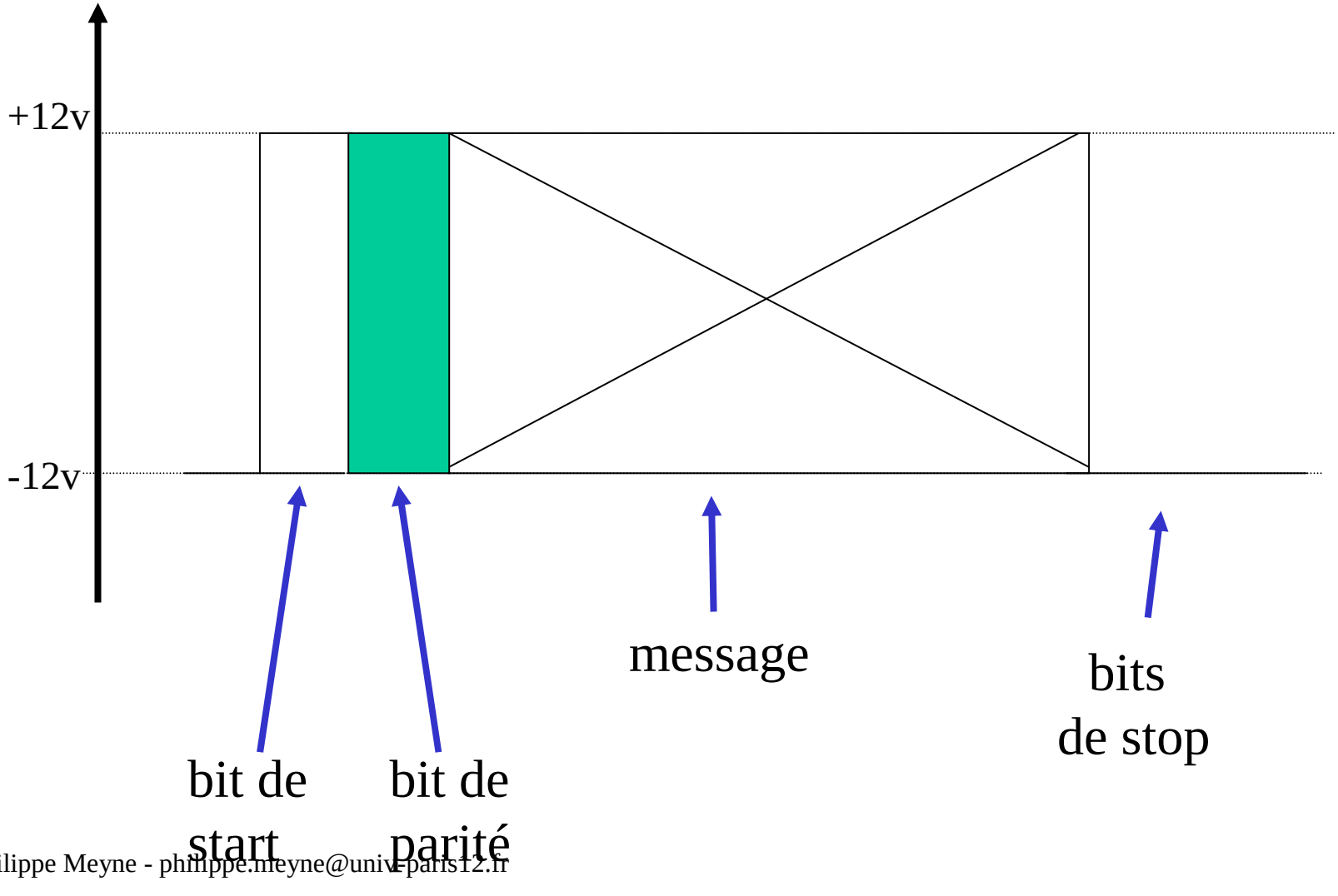
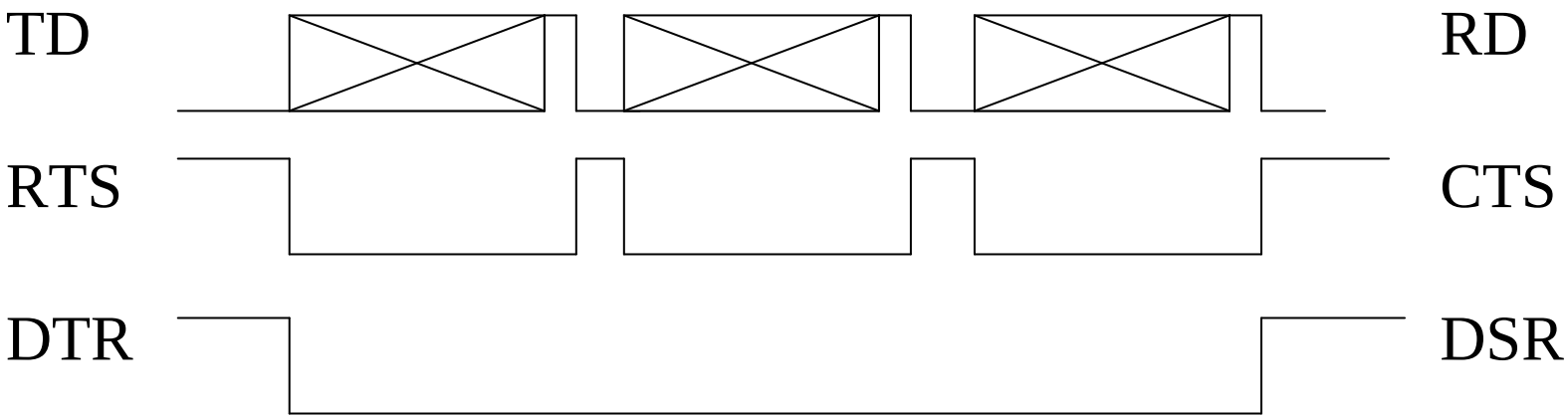


Format des données

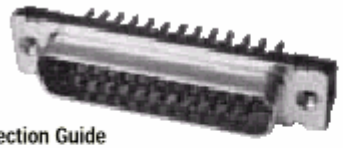


Signaux de contrôle



Connecteurs

Plug



Selection Guide

For Product Features, Specifications, Materials and Finishes, see pages 2-3.

Reader's Resource

For contact cavity arrangements, see page 224.
For P.C. hole patterns, see page 274.
For panel cutouts, see page 221.

Part Numbers

Shell Size	Layout	Through Hole	Clinch Nut # 4-40 UNC	Clinch Nut M3	Press-In Bolt # 4-40 UNC	Press-In Bolt M3
DE	9	DENG9P-P1	DENGE9P-P1	DENGX9P-P1	DENGZ9P-P1	DENGL9P-P1
DA	15	DANG15P-P1	DANGE15P-P1	DANGX15P-P1	DANGZ15P-P1	DANGL15P-P1
DB	25	DBNG25P-P1	DBNGE25P-P1	DBNGX25P-P1	DBNGZ25P-P1	DBNGL25P-P1
DC	37	DCNG37P-P1	DCNGE37P-P1	DCNGX37P-P1	DCNGZ37P-P1	DCNGL37P-P1
DD	50	DDNG50P-P1	DDNGE50P-P1	DDNGX50P-P1	DDNGZ50P-P1	DDNGL50P-P1

Note: For performance class 1 (gold over PdNi finish) add -408. Example: DENG9P-P1-408.

Specifications

Current Rating	5 A / 25°C, 3.5 A / 70°C ambient
Temperature Rating	−55°C to 125°C
Contact Resistance	10 mΩ
Test Voltage	1200 Vrms at Sea Level
Ø Plated Through Hole	1,09 - 0,94 (.043 - .037)
PC Tail Press-in Force	100N/contact max.
PC Tail Push-out Force	30N/contact min.
PC Board Thickness	3,20 - 1,60 (.125 - .062)

Materials and Finishes

Description	Material	Finish
Shell	Steel	Tin
Insulator	Thermoplastic, UL 94V-0	None (color: black)
Contact	Copper Alloy	Gold over Nickel (Standard) or Gold over PdNi (-408)
Hardware	Steel/Copper Alloy	Tin/Zinc

Connecteur - Brochage

broche	signal	signification
1	CD	Carrier Detect
2	RD	Received Data
3	TD	Transmitted Data
4	DTR	Data Terminal Ready
5	SG	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request to Send
8	CTS	Clear To send
9	RI	Ring Indicator

connecteur 9 broches

Broche	Signal
1	GND
2	RD
3	TD
4	CTS
5	RTS
6	DSR
7	SG
8	CD
9	
10	
11	
12	SCD
13	SRTS
14	SRD
15	TC
16	STD
17	RC
18	LL
19	SCTS
20	DTR
21	RL
22	RI
23	DSRS
24	ETC
25	TM

connecteur 25 broches

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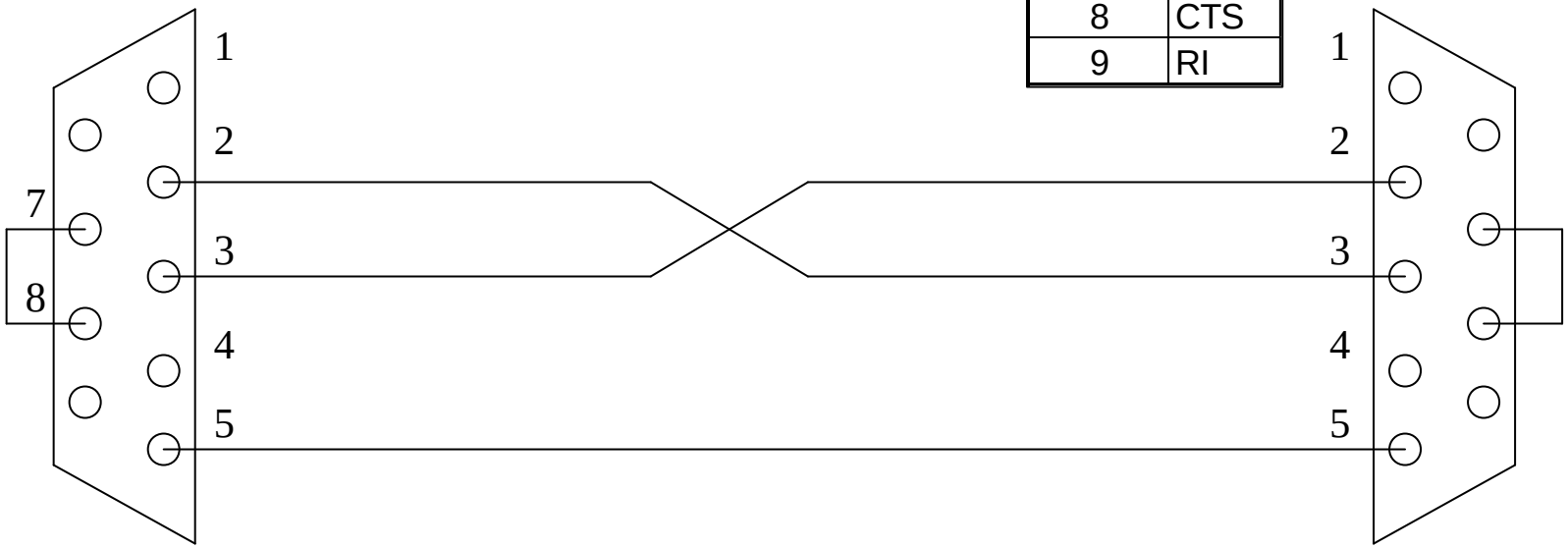
Liaison DTE - DTE trois fils

broche	signal
1	CD
2	RD
3	TD
4	DTR
5	SG
6	DSR
7	RTS
8	CTS
9	RI



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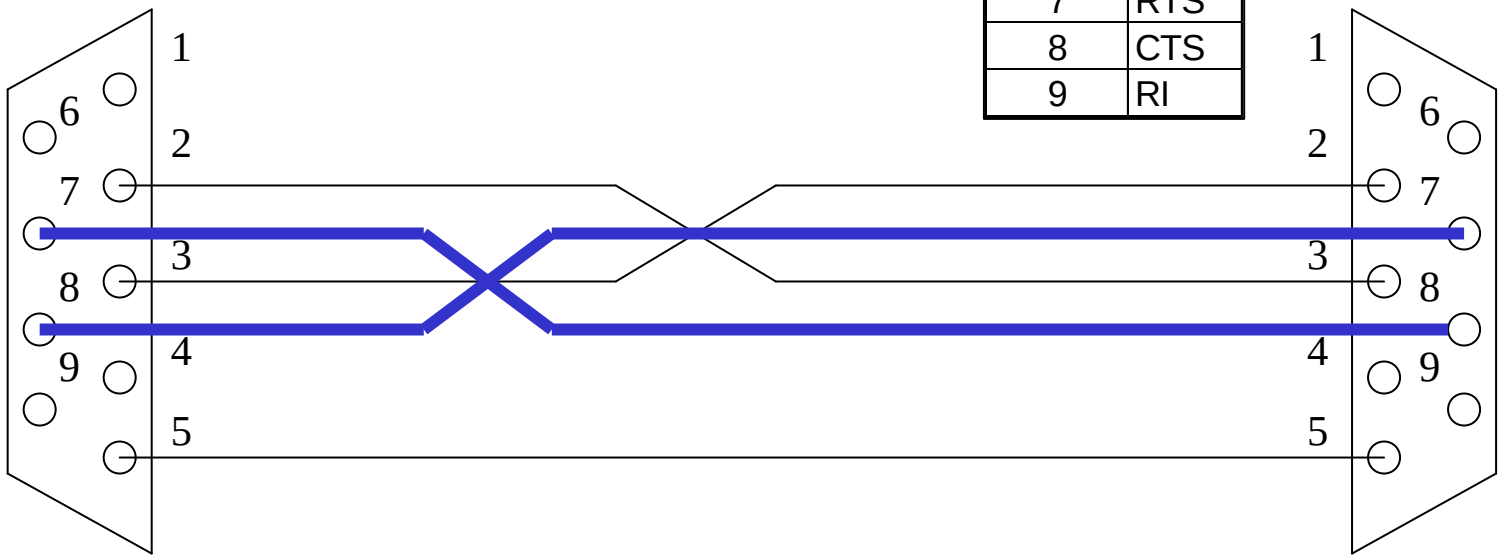
Liaison DTE - DTE cinq fils

broche	signal
1	CD
2	RD
3	TD
4	DTR
5	SG
6	DSR
7	RTS
8	CTS
9	RI



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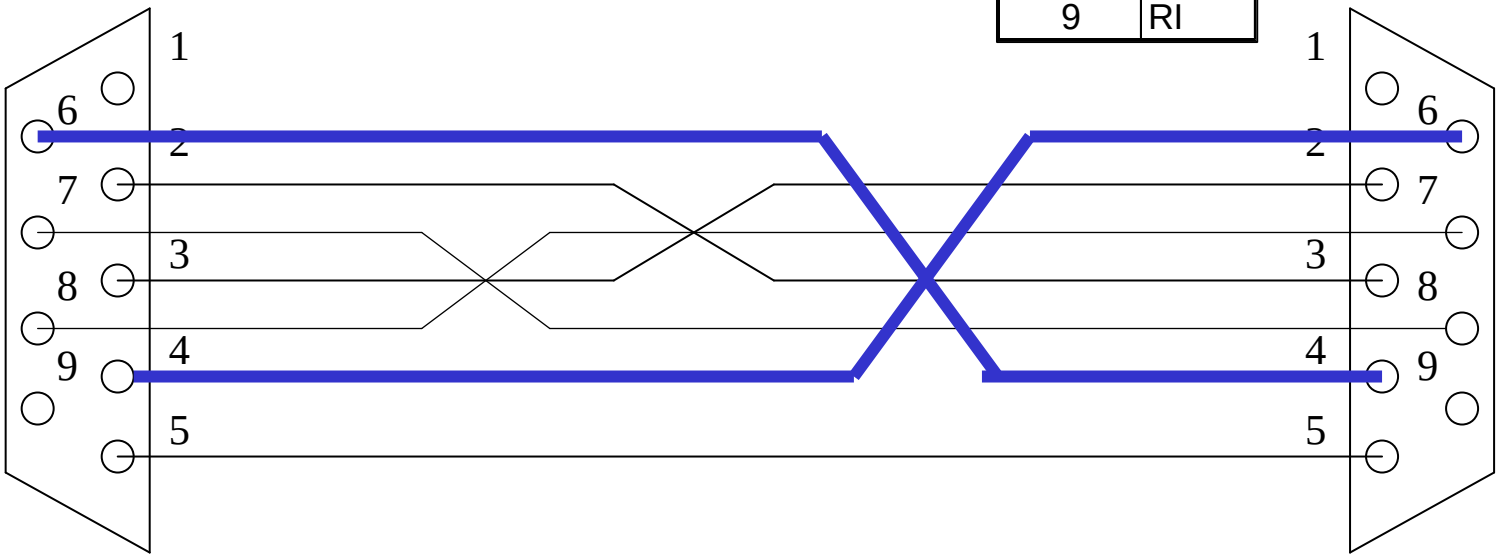
Liaison DTE - DTE sept fils

broche	signal
1	CD
2	RD
3	TD
4	DTR
5	SG
6	DSR
7	RTS
8	CTS
9	RI



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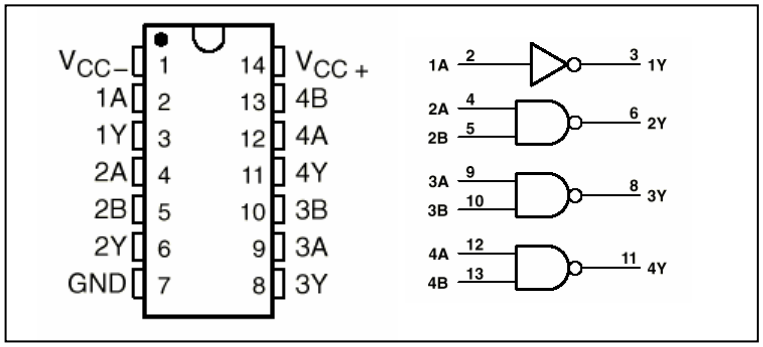
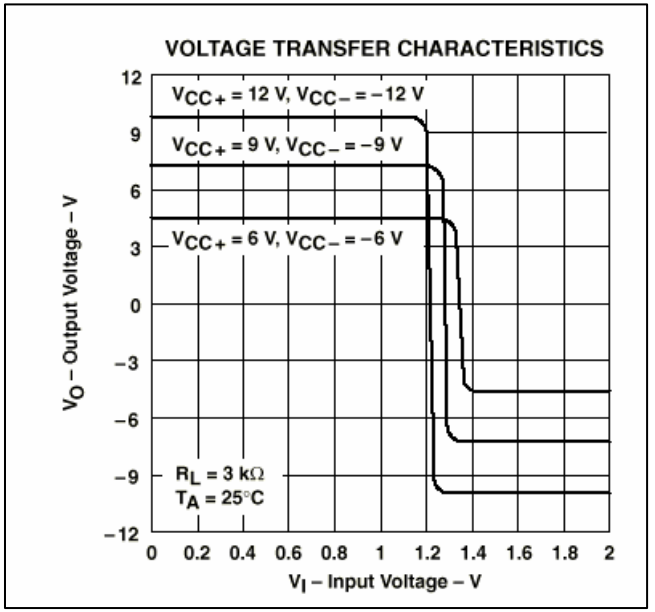
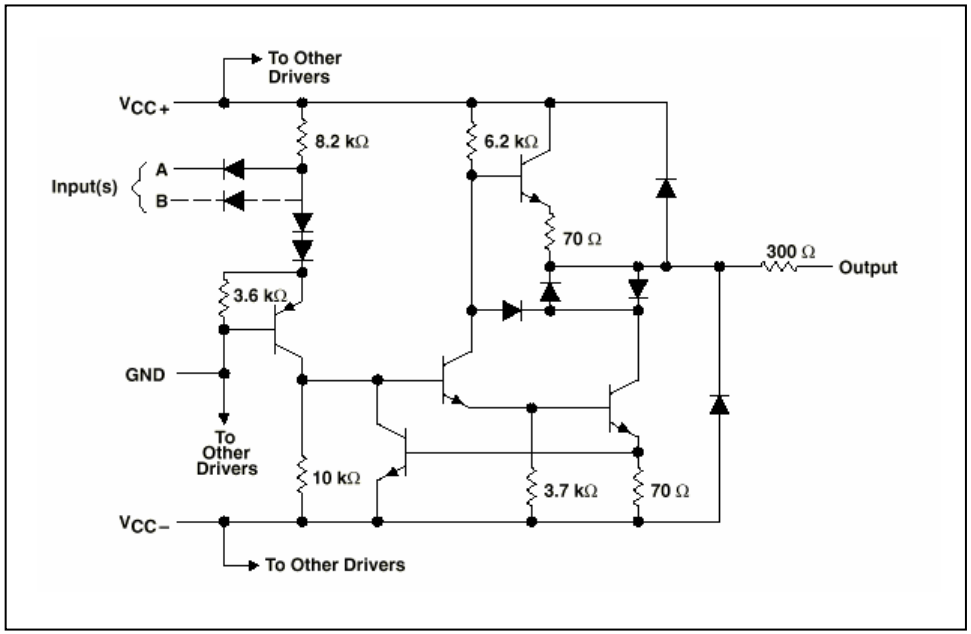
Mise en œuvre - Driver de lignes 1488







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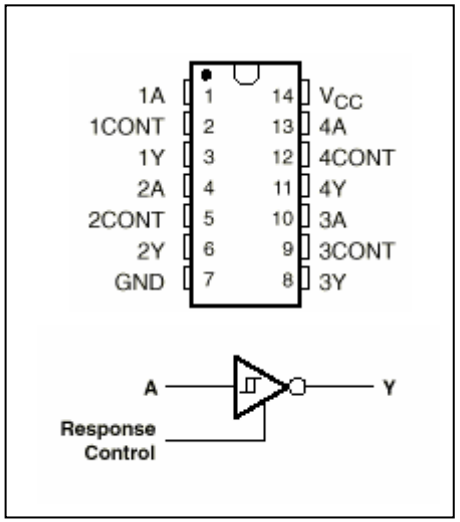
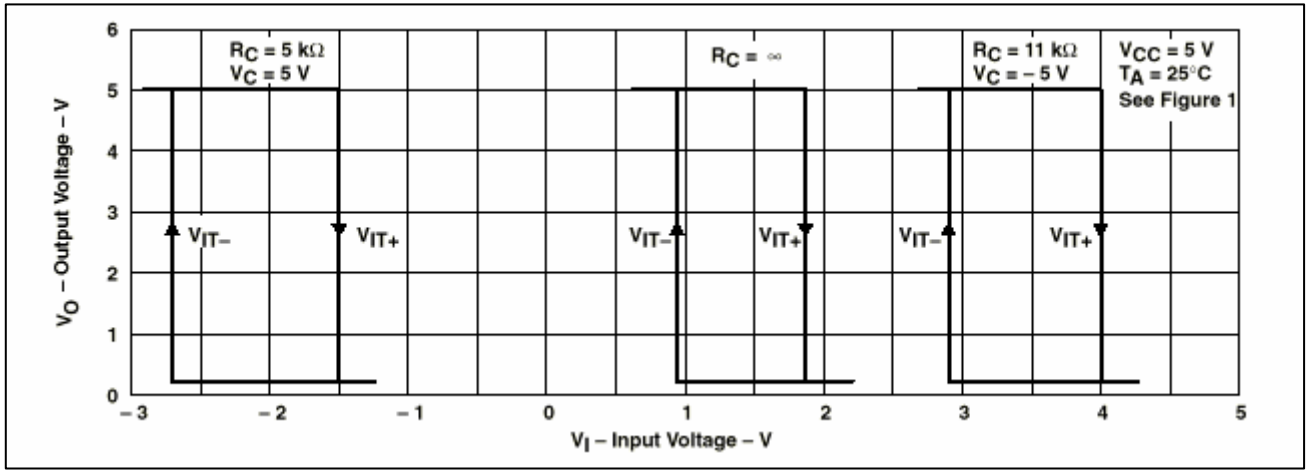
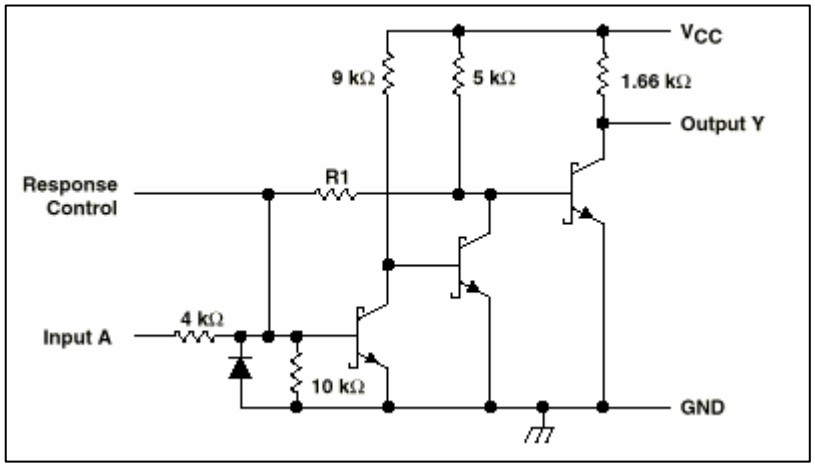
Mise en œuvre - Driver de lignes 1489







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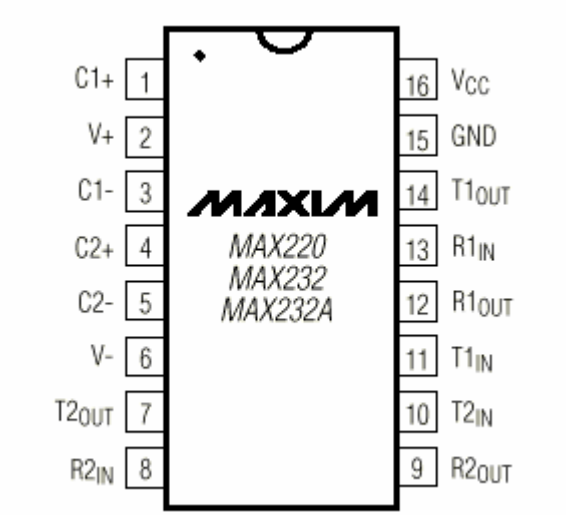
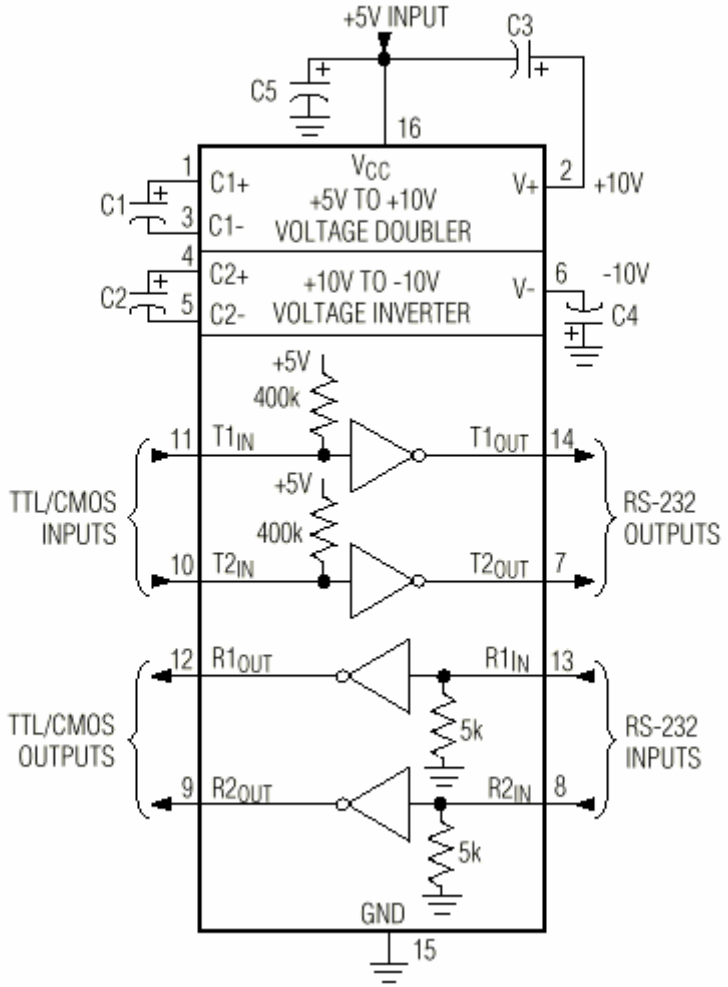
Mise en œuvre - Drivers MAX232





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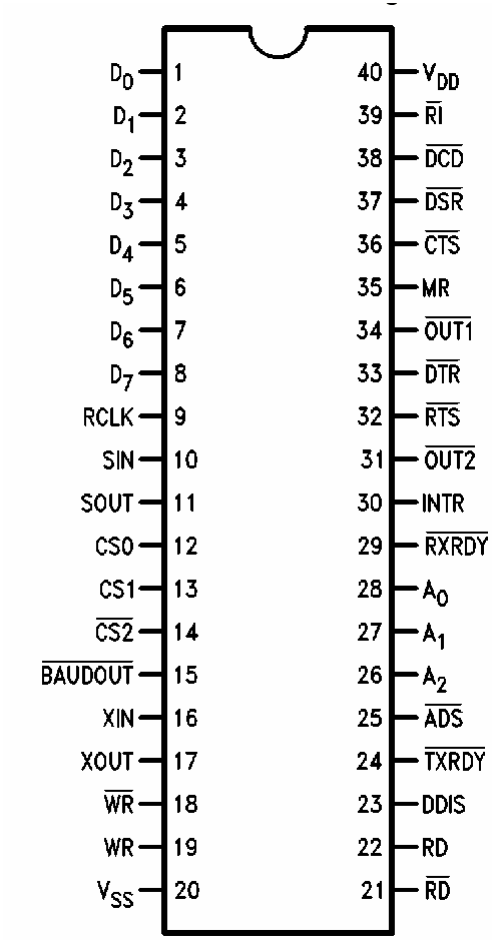
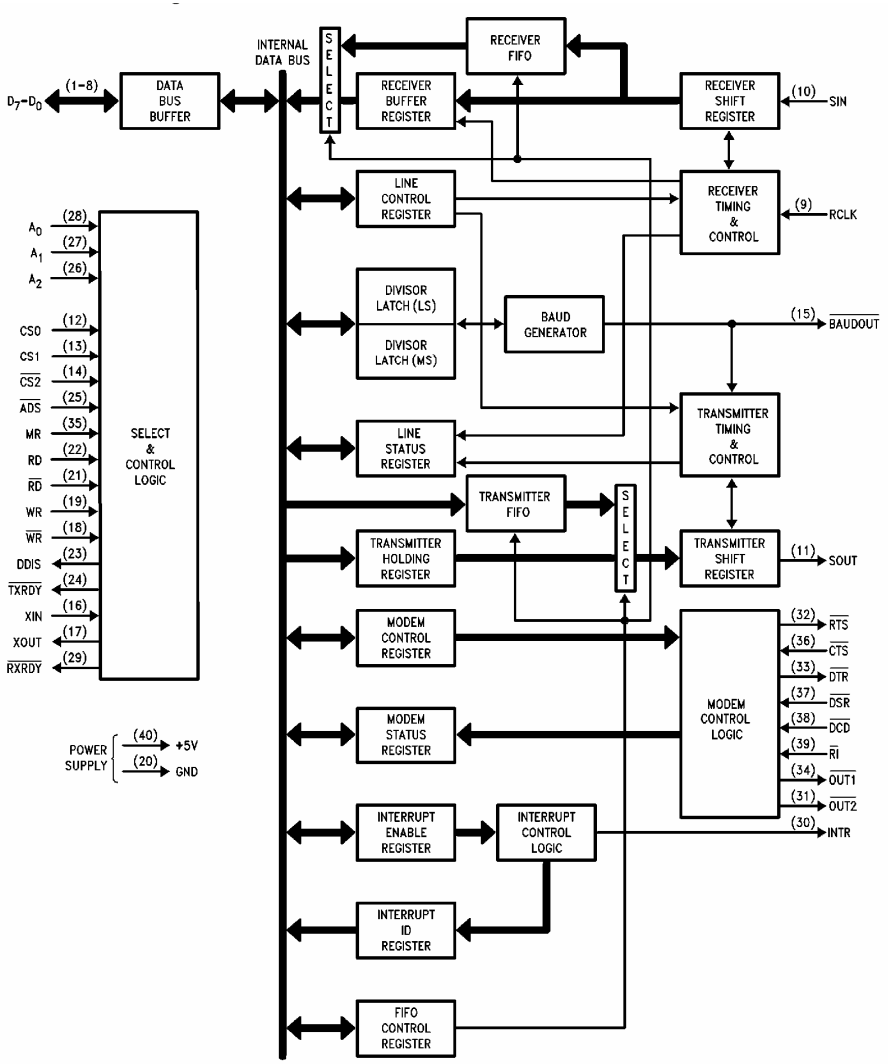
Mise en œuvre - UART - 8251/16550 Intel
Brochage – Structure interne





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Mise en œuvre - UART - 8251/16550 Intel
Registres

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

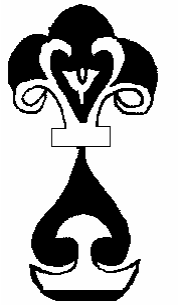
Mise en œuvre - UART - 8251/16550 Intel
Contenu des registres

TABLE II. Summary of Registers

Bit No.	Register Address											
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Reg-ister	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the 16450 Mode.



Mise en œuvre - UART - 8251/16550 Intel
Vitesse de la liaison série

Vitesse normalisée (bauds)	Divisor Latch High	Divisor Latch Low
50	0x09	0x00
75	0x06	0x00
110	0x04	0x17
150	0x03	0x00
300	0x01	0x80
600	0x00	0xC0
1200	0x00	0x60
2400	0x30	0x00
3600	0x00	0x20
4800	0x00	0x18
7200	0x00	0x10
9600	0x00	0x0C
19200	0x00	0x06
38400	0x00	0x03
57600	0x00	0x02
115200	0x00	0x01

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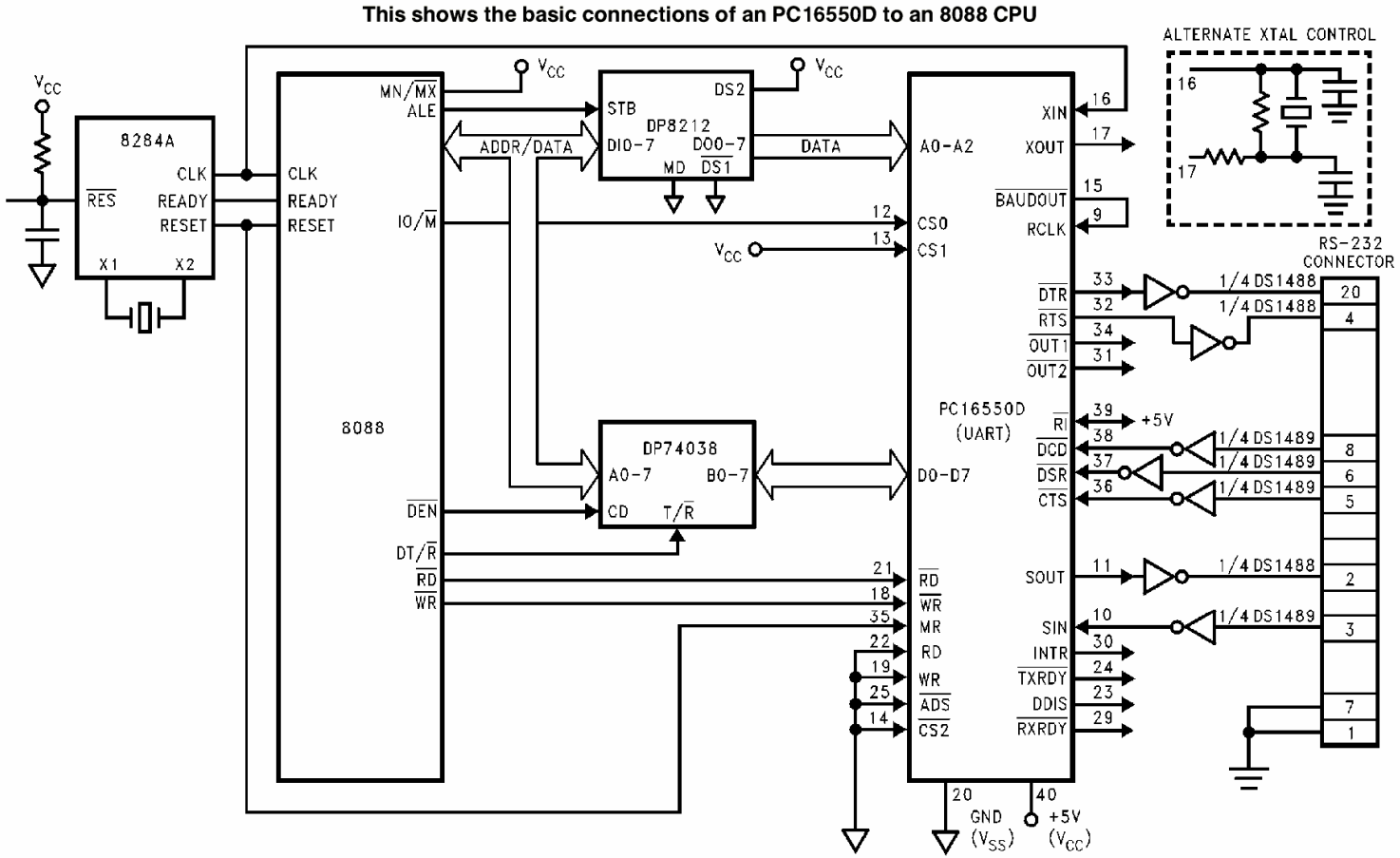
Mise en œuvre - UART - 8251/16550 Intel
Câblage



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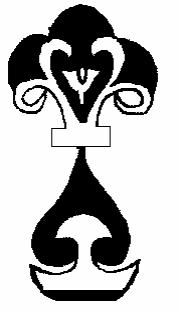
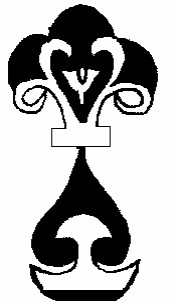


Mise en œuvre - UART - 8251/16550 Intel
Adresse des registres

Adresse	R/W	DLAB	Nom	Fonction
3F8h	R	0	RBR	Tampon de réception
3F8h	W	0	THR	Tampon d'émission
3F8h	R/W	1	DLL	Diviseur poids faible
3F9h	R/W	1	DLM	Diviseur poids fort
3F9h	R/W	0	IER	Autorisation interruption
3FAh	R	0	IIR	Identification interruption
3FAh	W	0	FCR	Commande FIFO
3FBh	R/W	0	LCR	Commande de la ligne série
3FCh	R/W	0	MCR	Commande du modem
3FDh	R	0	LSR	Etat de la ligne
3FEh	R	0	MSR	Etat du modem

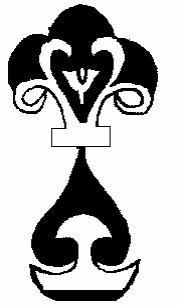


Mise en œuvre - UART - 8251/16550 Intel
Programmation sous LINUX – Structure termios

tcflag_t *c_iflag*; /* modes d'entrée */
tcflag_t *c_oflag*; /* modes de sortie */
tcflag_t *c_cflag*; /* modes de contrôle */
tcflag_t *c_lflag*; /* modes locaux */
cc_t *c_cc*[**NCCS**]; /* caractères de controle */

Mise en œuvre - UART - 8251/16550 Intel
Programmation sous LINUX – Exemple 1

```
int fd;
struct termios tty;
/* Ouverture de la liaison série*/
fd = open(« /dev/ttyS0 », O_RDWR);
/* Lecture des paramètres */
tcgetattr(fd, &tty);
tcgetattr(fd, &old);
/* changement de la vitesse */
cfsetospeed(&tty, B19200);
cfsetispeed(&tty, B19200);
/* On applique le nouveau paramétrage */
tcsetattr(fd, TCSANOW, &tty);
```



Mise en œuvre - UART - 8251/16550 Intel
Programmation sous LINUX – Exemple 2

```
tcgetattr(fd, &term);
/* mode RAW, pas de mode canonique, pas d'écho */
term.c_iflag = IGNBRK;
term.c_lflag = 0;
term.c_oflag = 0;
/* Controle de flux hardware (RTS/CTS) */
term.c_cflag |= (CREAD | CRTSCTS);
/* 1 caractère suffit */
term.c_cc[VMIN] = 1;
/* Donnée disponible immédiatement */
term.c_cc[VTIME] = 0;
/* 8 bits de données, pas de parité */
term.c_cflag &= ~(PARENB | CSIZE);
term.c_cflag |= CS8;
/* /* On applique le nouveau paramétrage */
tcsetattr(fd, TCSANOW, &term);
```

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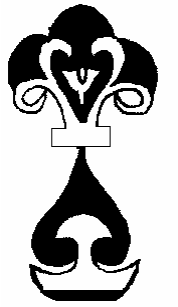
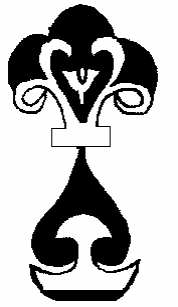


Mise en œuvre - UART - 8251/16550 Intel
Programmation sous Windows

```
HANDLE g_hCOM;
/* GENERIC_READ|GENERIC_WRITE   : autorisation de lire et d'écrire */
/* 0 : interdiction de partage du fichier */
/* NULL : Pointeur vers une structure SECURITY_ATTRIBUTES qui spécifie */
          les attributs de sécurité du fichier */
/* OPEN_EXISTING : Ouvre le fichier. S'il n'existe pas, la fonction échoue */
/* FILE_ATTRIBUTE_SYSTEM  : Fichier système */
/* NULL : Clé offrant un accès GENERIC_READ à un fichier modèle. */
          Ce dernier fournit des attributs étendus au fichier en cours de création */

g_hCOM = CreateFile(szCOM, GENERIC_READ|GENERIC_WRITE, 0, NULL,
                    OPEN_EXISTING, FILE_ATTRIBUTE_SYSTEM, NULL);

/*Code de retour : Handle du fichier ouvert */
if(g_hCOM == INVALID_HANDLE_VALUE)
{         printf("Erreur lors de l'ouverture du port COM");
          exit(0);
}
```



Mise en œuvre - UART - 8251/16550 Intel
Programmation sous Windows

```
// Configuration du Port
        …
      g_dcb.BaudRate = 9600;
      g_dcb.fParity = false;
      g_dcb.fDtrControl = DTR_CONTROL_ENABLE;
      g_dcb.ByteSize = 8;
      g_dcb.Parity = NOPARITY;
      g_dcb.StopBits = ONESTOPBIT;
        …
    SetCommState(g_hCOM, &g_dcb);
```

Conclusion

- Liaison ancienne mais toujours d’actualité
- Liaison simple, supporté par beaucoup de système
- Remplacée par USB, reste souvent en secours
- Support de beaucoup de RLI : MODBUS etc ….